escape of the above-mentioned impurity and after consideration thereof, the inventor has reached such an idea to form a required minimum local low permittivity region only at a portion being the most effective in reducing the fringe capacitance. Since the fringe capacitance is parasitic capacitance generated mainly between a gate electrode end and a semiconductor substrate, the low permittivity region may be formed at a side lower portion of the gate electrode, that is, the most responsible portion for generating this parasitic capacitance.

[0024] First Aspect

[0025] Here, as shown in **FIG. 1**, a MOS transistor has a gate electrode **3** formed on a semiconductor substrate **1** via a gate insulation film **2**, and a source **4** and a drain **4** formed on both sides of the gate electrode **3**, wherein, with sidewall films **5** each consisting of two layers (a thin first film **5***a* and a second film **5***b* for covering the first film **5***a*), a lower part of the first film **5***a*, that is, only a side lower portion of the gate electrode **3** becomes a local low permittivity region to be filled in with a low permittivity material **6**, and then the second film **5***b* is formed to cover the low permittivity material **6**.

[0026] Second Aspect

[0027] Here, as shown in **FIG. 2**, in a MOS transistor similar to that in **FIG. 1**, with sidewall films **5** each consisting of two layers (a thin first film **5***a* and a second film **5***b* for covering the first film **5***a*), the first film **5***a* is formed only at a side upper portion of the gate electrode **3**, while only a side lower portion of the gate electrode **3** becomes a low permittivity region. Then, the second film **5***b* is formed with low step coverage so as not to fill in the region, to thereby form a local cavity **7** surrounded by the sidewall films **5**.

[0028] Third Aspect

[0029] Here, as shown in **FIG. 3**, in a MOS transistor similar to that in **FIG. 1**, a part of side wall lower portions (and a gate insulation film **2**) of a gate electrode **3** is removed by etching to make it notch-shaped. Then, this portion becomes a local low permittivity region to be filled in with a low permittivity material **6**, and then sidewall films **8** are formed to surround it.

[0030] Fourth Aspect

[0031] Here, as shown in **FIG. 4**, in a MOS transistor similar to that in **FIG. 1**, a part of side wall lower portions (and a gate insulation film **2**) of a gate electrode **3** is removed by etching to make it notch-shaped. Then, this portion becomes a local low permittivity region and sidewall films **8** are formed with low step coverage so as not to fill in the local low permittivity region, to thereby form a local cavity **7** surrounded by the sidewall films **8**.

[0032] Japanese Patent Laid-open No. Hei 4-152535 discloses a semiconductor device composed of a high dielectric film at a lower portion of sidewall films and a low dielectric film at an upper portion thereof. An object thereof is to attempt having even lower electric field at an LDD part and reducing the parasitic capacitance between the gate and wiring. Therefore, the disclosed invention totally differs from the present invention not only in its structure, but also in its objects and effect.

[0033] Specific Various Embodiments

[0034] Based on the contents of the above-described main points of this invention, various preferred embodiments, to which this invention is applied, are described in detail with reference to the drawings.

[0035] First Embodiment

[0036] This embodiment discloses a structure of a semiconductor device that has a MOS transistor structure having a gate electrode, a source, and a drain, and a method for manufacturing the same. Here, the MOS transistor structure is explained together with its manufacturing process for convenience.

[0037] **FIGS. 5A** to **5**G are schematic sectional views showing, in a process order, a method for manufacturing the MOS transistor relating to this embodiment.

[0038] First, as shown in **FIG. 5A**, a polycrystalline silicon film (not shown) is deposited on, for example, a p-type silicon semiconductor substrate **11** via a gate insulation film **12** by a CVD method or the like, and patterning of the polycrystalline silicon film and the gate insulation film **12** into an electrode shape causes to form a gate electrode **13**.

[0039] Next, as shown in **FIG. 5B**, for example, a silicon oxide film (not shown) is deposited on the semiconductor device **11** by the CVD method or the like to cover the gate electrode **13**, and full anisotropic etching (etch back) of this silicon oxide film causes to form thin first films **14***a* only on side surfaces of the gate electrode **13** and the gate insulation film **12**.

[0040] Next, as shown in **FIG. 5C**, only lower portions of the first films **14***a* are selectively removed by, for example, wet etching, to expose surfaces on side lower portions of the gate electrode **13**. Here, the exposed side lower portions of the gate electrode **13** become low permittivity regions **15**.

[0041] Next, as shown in **FIG. 5D**, ion implantation of an n-type impurity such as phosphorus (P) is performed using the gate electrode **13** and the first films **14***a* as masks, to form a pair of extension regions **16** on a surface layer of the semiconductor substrate **11**.

[0042] Next, as shown in **FIG. 5E**, a low permittivity material **21** is formed on the gate electrode **13** with the low permittivity regions **15** being filled in, and etching (for example, etch back) thereof causes to leave the low permittivity materials **21** only in the low permittivity regions **15**. Here, such low permittivity materials are used for the low permittivity material **21** as a SiOF, an arylether based organic low permittivity material, a fluorocarbon based low permittivity material, a hydrogen silses quioxane based low permittivity material, a hydromethyl silses quioxane based low permittivity material, a porous quioxane based low permittivity material, a porous allylether based low permittivity material, or the like.

[0043] Next, as shown in **FIG. 5F**, for example, a silicon nitride film (not shown) is deposited by the CVD method or the like to cover the gate electrode **13**, and thereafter the full anisotropic etching (etch back) of this silicon nitride film causes to form second films **14***b* that cover side surfaces of the first films **14***a* and the low permittivity regions **15** filled with the low permittivity material **21**. Thereby, sidewall